17.1

Single instruction, single data (SISD) stream architecture: The control unit(CU) of the processing unit (PU) will execute a single instruction stream (IS) in order to perform the operations on the data stored in a single memory unit (MU).

Single instruction, multiple data (SIMD) stream architecture: A single machine instruction can control the execution of multiple processing elements simultaneously.

Multiple instructions, multiple data (MIMD) stream architecture: A set of processors executing different set of instruction sequences on different data sets simultaneously

17.2

There are two or more processors that are having equal capabilities

These processors are sharing the same main memory and Input-Output (I/O) devices.

These processors are interconnected with a system bus so that the access time of memory is same for every processor.

All processors can have access to I/O devices whether it may be through same path or other.

As it is a parallel processing technique a function can be done by all the multiprocessors parallel.

The Operating System presents in the system controls the system and provides interaction between processors and their jobs.

The Operating System of an SMP is responsible for scheduling the processes or threads across all processors.

17.3

Performance

Availability

Incremental growth

Scaling

17.4

Simultaneous concurrent processes

Scheduling

Synchronization

Memory management

Reliability and fault tolerance

17.5

Software cache coherent schemes: Attempt to avoid the need for additional hardware circuitry and logic by relying on the compiler and operating system to deal with the problem

Hardware cache coherent schemes: Hardware-based solutions are generallyreferred to as cache coherence protocols. These solutions provide dynamic recognition at run time of potential inconsistency conditions. Because the problem is only dealt with when it actually arises, there is more effective use of caches, leading to improved performance over a software approach. In addition, these approaches are transparent to the programmer and the compiler, reducing the software development burden.

17.6

Modified: The line in the cache has been modified and is available only in this cache

Exclusive: The line in the cache is the same as that in main memory and is not present in any other cache

Shared: The line in the cache is the same as that in main memory and may be present in another cache

Invalid: The line in the cache does not contain valid data